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Steve M. Perry
THORPE, NORTH & WESTERN, LLP
P.O. Box 1219
Sandy, UT 84091-1219

EXAMINER	
PRENDERGAST, ROBERTA D	
ART UNIT	PAPER NUMBER
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/694,411	GARDINER ET AL.	
	Examiner	Art Unit	
	Roberta Prendergast	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-14 and 24-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-14 and 24-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 25, 30, 31, 33 and 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 25 depends from claim 24 and incorporates all the limitations contained therein, thus the limitation of "initiating the displaying of the screen bins rendered after at least one row of screen bins has completed rendering" is in direct contradiction to the limitation of "displaying at least one rendered screen bin when the rendering of the screen bins for the one single pixel frame buffer is at least ½ completed" thus rendering dependent claim 25 indistinct as it is unclear as to whether the displaying step should be initiated after the rendering of at least one row of screen bins or after the rendering is at least ½ completed.

Claims 33 and 37 depend from claims 32 and 36 and are rendered indistinct for the reasons provided for claim 25 above.

Claims 30 and 31, which ultimately depend from claim 24 and incorporate all the limitations contained therein are rendered indistinct because the limitation of utilizing a double-buffered pixel frame memory is in direct contradiction to the limitation of a single pixel frame buffer.

Claim 34 recites the limitation "a geometry engine configured to transform the database and the primitives used by the image generator" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 35 recites the limitation "a real-time controller configured to receive real-time control information and compute the transformation matrices" in lines 1-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim 10, 11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Kajiya et al. U.S. Patent No. 5864342.

Referring to claim 10, Kajiya et al. teaches a method for enabling a single pixel frame buffer (column 6, lines 15-29, i.e. a single rasterization buffer is understood to be a single pixel frame buffer) for simultaneous rendering and display in a computer image generator comprising the steps of a) dividing a geometry buffer into a plurality of screen bins (column 10, lines 35-42, i.e. the scene/image is divided into pixel regions called chunks and the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into); (b) storing primitives in each screen bin the primitives touch (column 10, lines 40-44; columns 15-16, lines 59-2, i.e. the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into and geometry that overlaps a chunk boundary is referenced in each chunk it is visible in); (c) rendering the screen bins by row from top to bottom, into the pixel frame buffer (column 8, lines 45-49; column 41, lines 20-27, i.e. the chunks are rendered from left-to-right, top-to-bottom scan order); and (d) displaying at least one row of screen bins rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins takes place after a selected portion of the screen bins for a current field have been rendered (column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row of screen bins/chunks has completed rendering and while a second row of screen bins/chunks is being rendered such that the selected portion of screen bins

rendered prior to the initiation of the display step is understood to be one row/band of screen bins/chunks).

Referring to claim 11, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10, further comprising the step of reducing the transport delay without allowing the display step to overlap a rendering envelope (Fig. 22; column 56, lines 11-40).

Referring to claim 13, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10 further comprising the step of rendering at least one row of screen bins before the display step begins (column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row has completed rendering).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya et al. in view of Grigor et al. U.S. Patent No. 6853381.

Referring to claim 12, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10 but does not specifically teach the

step of reducing the transport delay and allowing the display step to overlap a rendering envelope.

Grigor et al. teaches this limitation (Abstract; Figs. 1 and 8; column 3, lines 13-33; column 8, lines 32-67, i.e. individual display lines comprising a plurality of pixels are rendered and stored in the frame buffer in a memory location only if the location has been previously accessed for display).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kajiya et al. to include the teachings of Grigor et al. thereby overcoming the problems associated with single frame buffers such as tearing, choppy video/graphics and stalling (columns 1-2, lines 32-13) by allowing the frame buffer to be utilized more efficiently (column 3, lines 46-50) and allowing for an efficient way to receive primitives to be displayed, while assuring the data integrity of the frame buffer (columns 9-10, lines 66-10).

Referring to claim 14, the rationale for the rejection of claim 10 is incorporated herein, Kajiya et al. teaches a method as in claim 10 further comprising but does not specifically teach the step of reducing the transport delay by allowing the display step to overlap a rendering envelope without allowing pixels from a previous field to be displayed.

Grigor et al. teaches this limitation (Abstract; Figs. 1 and 8; column 3, lines 13-33; column 5, lines 13-25 and 56-67; column 8, lines 32-67, i.e. individual display lines comprising a plurality of pixels are rendered and stored in the frame buffer in a memory location only if the location has been previously accessed for display and the PIXEL

OFFSET and LINE INDICATOR are utilized to prevent the display of previously displayed pixels).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kajiya et al. to include the teachings of Grigor et al. thereby overcoming the problems associated with single frame buffers such as tearing, choppy video/graphics and stalling (columns 1-2, lines 32-13) by allowing the frame buffer to be utilized more efficiently (column 3, lines 46-50) and allowing for an efficient way to receive primitives to be displayed, while assuring the data integrity of the frame buffer (columns 9-10, lines 66-10).

Claims 24-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya et al. in view of Taraci et al. U.S. Patent No. 6316974 .

Referring to claim 24, Kajiya et al. teaches a method for enabling a single pixel frame buffer (column 6, lines 15-29, i.e. a single rasterization buffer is understood to be a single pixel frame buffer) for simultaneous rendering and display in a computer image generator comprising the steps of a) dividing a geometry buffer into a plurality of screen bins (column 10, lines 35-42, i.e. the scene/image is divided into pixel regions called chunks and the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into); (b) storing primitives in each screen bin the primitives touch (column 10, lines 40-44; columns 15-16, lines 59-2, i.e. the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into and geometry that overlaps a chunk boundary is referenced in each chunk it is visible in); (c) rendering the

screen bins by row from top to bottom, into the pixel frame buffer (column 8, lines 45-49; column 41, lines 20-27, i.e. the chunks are rendered from left-to-right, top-to-bottom scan order) but does not specifically teach (d) displaying at least one rendered screen bin when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed.

Taraci et al. teaches this limitation (column 8, lines 30-45, i.e. the output/display vertical frame read pointer is placed at a point in reference to the input/render vertical write pointer to create a frame rate delay of ½ a frame indicating that rendering is at least ½ completed before displaying begins).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kajiya et al. to include the teachings of Taraci et al. thereby providing a system capable of locking the output vertical frame sync pulses to the input vertical frame sync pulses where the read and write pointers do not cross and where it does not produce an output frame made up of two different input frames (Taraci et al.: column 8, lines 25-34 and 46-66).

Referring to claim 25, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al. teaches a method as in claim 24, wherein step (d) further comprises the step of initiating the displaying of the screen bins rendered after at least one row of screen bins has completed rendering (Kajiya et al.: column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row has completed rendering).

Referring to claim 30, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al. teaches a method as in claim 24, further comprising the step of utilizing a double buffered pixel frame memory (column 6, lines 30-40 and 55-59; column 8, lines 43-51; column 13, lines 54-64; column 14, lines 31-37; column 17, lines 34-48, i.e. the pixel frame memory can be a double buffer memory that can be toggled between input and output activities thus allowing processing tasks to be performed without adding delay in the rendering pipeline), wherein an input side and output side of the double buffered pixel frame memory toggle independently (column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row has completed rendering indicating that the input and output side are toggled independently).

Referring to claim 31, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al., as modified by Taraci et al. above, teaches a method as in claim 24, further comprising the step of utilizing a double buffered frame memory (column 6, lines 30-40 and 55-59; column 8, lines 43-51; column 13, lines 54-64; column 14, lines 31-37; column 17, lines 34-48, i.e. the pixel frame memory can be a double buffer memory that can be toggled between input and output activities thus allowing processing tasks to be performed without adding delay in the rendering pipeline), wherein the input side and output side of the double buffered frame memory toggle independently (column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row has completed rendering indicating that the input and output side are

toggled independently) and the rendering step is at least one half of a field ahead of the display step (Taraci et al.: column 8, lines 30-45, i.e. the output/display vertical frame read pointer is placed at a point in reference to the input/render vertical write pointer to create a frame rate delay of ½ a frame indicating that rendering is at least ½ of a frame ahead of the display step). Therefore the motivation for combining the method of Kajiya et al. with the teachings of Taraci et al. as written for claim 24 above is incorporated herein.

Referring to claim 32, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al. teaches an image generator with a single pixel frame buffer enabled for simultaneous rendering and display comprising a geometry buffer, a rendering engine, and a display processor for performing the method of claim 24 (Figs. 1-4B and 9-14).

Referring to claim 33, claim 33 recites the elements of claims 25 and 32 and therefore the rationale for the rejection of claims 25 and 32 are incorporated herein.

Referring to claim 34, the rationale for the rejection of claim 32 is incorporated herein, Kajiya et al. teaches a method as in claim 32, further comprising a geometry engine configured to transform the database and the primitives used by the image generator (Figs. 1, 4A and 4B; column 15, lines 59-67).

Referring to claim 35, the rationale for the rejection of claim 32 is incorporated herein, Kajiya et al. teaches a method as in claim 32, further comprising a real-time controller configured to receive real-time control information and compute the transformation matrices (column 17, lines 4-9; column 61, lines 5-13).

Referring to claim 36, the rationale for the rejection of claim 32 is incorporated herein, Kajiya et al. teaches a method for reducing the transport delay in a computer image generator, comprising the steps of: (a) dividing a display screen into a plurality of screen bins which store every primitive that touches a screen region defined by the screen bin (column 10, lines 35-42, i.e. the scene/image is divided into pixel regions called chunks and the geometry is pre-sorted into screen bins, which represent the area of a display screen and stores every primitive that touches the screen region defined by that bin, based on which chunk the geometry will be rendered into); (b) rendering the primitives in the screen bins by row from top to bottom in a frame buffer (column 10, lines 40-44; columns 15-16, lines 59-2, i.e. the geometry is pre-sorted into bins based on which chunk the geometry will be rendered into and geometry that overlaps a chunk boundary is referenced in each chunk it is visible in); (c) displaying at least one screen bin rendered into the flame buffer when the rendering of the screen bins is at least 1/2 completed.

Referring to claim 37, claim 37 recites the elements of claims 25 and 36 and therefore the rationale for the rejection of claims 25 and 36 are incorporated herein.

Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya et al. in view of Taraci et al. as applied to claim 24, 25 and 36 above, and further in view of Grigor et al. U.S. Patent No. 6853381.

Referring to claim 26, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al. teaches a method as in claim 24, further comprising the step of

using a hardware interlock to ensure that the rendering step does not advance ahead of the display step (Kajiya: Fig. 22 (element 748); column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row has completed rendering; Grigor et al.: column 3, lines 18-37, i.e. a write behind controller is used to enable the rendering and display steps to be performed concurrently within a single pixel frame buffer).

Referring to claim 27, the rationale for the rejection of claim 26 is incorporated herein, Kajiya et al. teaches a method as in claim 26, further comprising the step of using a row based hardware interlock to ensure that the rendering step does not advance ahead of the display step (Kajiya: column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row has completed rendering; Grigor et al.: column 3, lines 18-37, i.e. a write behind controller is used to enable the rendering and display steps to be performed concurrently within a single pixel frame buffer).

Referring to claim 28, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al. teaches a method as in claim 24, further comprising the step of executing the rendering and displaying steps concurrently within the same frame buffer (Kajiya: column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, i.e. the step of displaying at least one row of screen bins is initiated after at least one row has completed rendering; Grigor et al.: column 3, lines 18-37, i.e. a write behind controller is used to enable the rendering and display steps to be performed concurrently within a single pixel frame buffer).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kajiya et al. to include the teachings of Grigor et al. thereby overcoming the problems associated with single frame buffers such as tearing, choppy video/graphics and stalling (columns 1-2, lines 32-13) by allowing the frame buffer to be utilized more efficiently (column 3, lines 46-50) and allowing for an efficient way to receive primitives to be displayed, while assuring the data integrity of the frame buffer (columns 9-10, lines 66-10).

Referring to claim 38, claim 38 recites the elements of claims 25, 27 and 36 and therefore the rationale for the rejection of claims 25, 27 and 36 are incorporated herein.

Claim 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiya et al. in view of Taraci et al. as applied to claim 24 above, and further in view of Regan U.S. Patent No. 6407736.

Referring to claim 29, the rationale for the rejection of claim 24 is incorporated herein, Kajiya et al. teaches a method as in claim 24 wherein the geometry/fragment buffers are double buffered (column 20, lines 53-63, i.e. fragment buffer is double buffered so that one fragment buffer could be resolved while the other is filled) but does not specifically teach wherein step (d) further comprises using an independent timer to control toggling of the geometry buffer.

Regan teaches this limitation (Figure 28 (elements 945 and 955); column 15, lines 15-22; columns 66-67, lines 45-60, i.e. a first triangle buffer 945 is used to write triangle data from the front end graphics processor while the second triangle buffer 955

is used to scan out data and the buffers are toggled/swapped at the end of the frame period, which is the time taken to write in the triangle data to one buffer and to scan out data from the other buffer).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kajiya et al. to include the teachings of Regan thereby allowing the front end processor to write the triangles of the next frame to one geometry buffer while scanning out the triangles of the current frame to the shader/texture mapping unit and thus limiting performance of the geometry buffer only by the time required to process each triangle and write triangle information into the triangle buffer (Regan: column 8, lines 44-55).

Response to Arguments

Applicant's arguments filed 11/28/2006 have been fully considered but they are not persuasive.

Applicant argues, with regards to claims 10, 11 and 13, "...Kajiya does not teach or suggest displaying at least one row of screen bins rendered before rendering of all the screen bins has been completed, as recited in independent claim 10. Rather, as previously discussed, Kajiya renders a scene using a tiler rendering engine 200, compresses the results, and stores the results in a memory 216. The stored results then undergo a geometric transformation 204 followed by post-processing 210 before being sent to a display...".

Examiner respectfully submits that Kajiya, column 6, lines 15-29; column 16, lines 15-25; column 60, lines 24-47 and 63-67; column 61, lines 11-13, teaches the step of displaying at least one row of screen bins is initiated after at least one row of screen bins/chunks has completed the rendering step and while a second row of screen bins/chunks is being rendered such that the selected portion of screen bins rendered prior to the initiation of the display step is understood to be one row/band of screen bins/chunks and wherein the geometry can be rendered to a common/single rasterization/frame buffer wherein pixel data generated while rasterizing primitives for a chunk are resolved before the next chunk in order to avoid the storage step as claimed.

Applicant argues, with regards to claims 10, 11 and 13, "...Kajiya teaches that the step of displaying is completed after each frame of the scene has been rendered, compressed, and stored. The two compositing buffers disclosed in column 61 occur in the post-processor 210 after the rendering engine 200 and geometric transformation engine 204. Thus, Kajiya does not disclose displaying at least one row of screen bins rendered before rendering of all the screen bins has been completed, as recited in claim 10. Rather, as taught in the abstract, Kajiya teaches that pixel-fragments can be resolved in a post-processing step for one chunk while primitives for another chunk are rasterized...".

Examiner respectfully submits that Kajiya, column 6, lines 15-29 and column 16, lines 15-25 teach wherein the geometry can be rendered to a common/single rasterization/frame buffer wherein pixel data generated while rasterizing primitives for a chunk are resolved before the next chunk in order to avoid the storage step as claimed.

Applicant then argues "...Further, Kajiya teaches double buffering even though the double buffers are smaller than conventional double buffers. This means that Kajiya teaches the use of a pixel frame buffer in combination with a smaller double buffered rendering area. This increases the frame buffer memory used by Kajiya by two screen band buffers or two chunk buffers, whereas the present invention uses only the single frame buffer...".

Examiner respectfully submits that Kajiya column 6, lines 15-29; column 60, lines 24-47 and 63-67; column 61, lines 11-13, teaches the step of displaying at least one row of screen bins is initiated after at least one row of screen bins/chunks has completed rendering and while a second row of screen bins/chunks is being rendered thus displaying at least one.

Applicant next argues "...The present invention does not use double buffering. Claim 24 (previously claim 1) includes the limitation of "enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator." This limitation is also included in paragraph (d) of claim 1. The prior art does not teach or suggest using a single pixel frame buffer...".

Examiner respectfully submits that applicant look to page 15 of the specification, original claims 8 and 9, and new claims 30 and 31, which specifically use a double buffered frame memory, thus contradicting applicant's argument.

Applicant's arguments with respect to new claims 24-38 are premature since the claims were not present and therefore were not rejected in the previous office action

mailed 8/28/2006. Please see the office action above for the Examiner's response to the new claims submitted in the amendment filed 11/28/2006.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberta Prendergast whose telephone number is (571) 272-7647. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RP 2/15/2007

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER